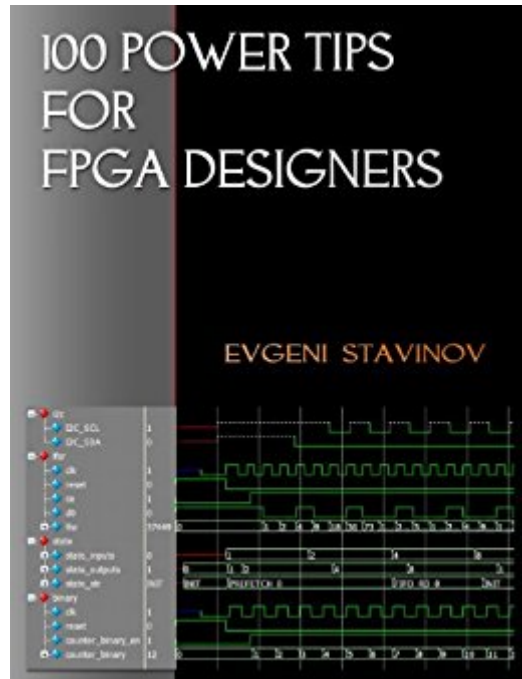The book was found

100 Power Tips For FPGA Designers

100 POWER TIPS
FOR
FPGA DESIGNERS

EVGENI STAVINOV

Synopsis

This book is a collection of short articles on various aspects of FPGA design: synthesis, simulation, porting ASIC designs, floorplanning and timing closure, design methodologies, performance, area and power optimizations, RTL coding, IP core selection, and many others. The book is intended for system architects, design engineers, and students who want to improve their FPGA design skills. Both novice and seasoned logic and hardware engineers can find bits of useful information.This book is written by a practicing FPGA logic designer, and contains a lot of illustrations, code examples, and scripts. Rather than providing information applicable to all FPGA vendors, this book edition focuses on Xilinx Virtex-6 and Spartan-6 FPGA families. Code examples are written in Verilog HDL. All code examples, scripts, and projects provided in the book are available on accompanying website.

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Customer Reviews

I was initially skeptical, thinking that this is like many other "N tips for XXX" books which enumerate all sorts of tips on a particular subject. This book is actually not like that. It is fairly well structured, and almost self-contained in one respect.I view this book as a fairly detailed presentation of the design methodology in the FPGA world. Discussions about engineering tradeoffs abound. I found the book easy to read beginning to end, but I think it's OK to skip the chapters/tips you don't need to read about. A good complement to this book is Advanced FPGA Design by Steve Kilts.My only complaint is that the book doesn't go deep enough in some subjects, and the Xilinx-heavy focus. Hopefully these will be improved in future editions.

I have been programming FPGAs for about 7 years. I'm not an expert though, and I thought that this book would have some useful info.Most of the the tips are very light on explanation. They might be useful as google fodder, but don't expect to really learn much from this book.

I have never worked with FPGAs before, but I'm now working with someone who has over 20 years of experience. Many of the things I've heard my associate talk about are discussed in good detail in the book. For example, the importance of pin assignment, the "art" of timing closure, and floor-planning the design. The book is easy-to-read, and since it's more of a "cookbook" style, you can open it pretty much anywhere and dig-in. The book is focussed on the Spartan-6 and Virtex-6 FPGAs from Xilinx (which is what we're using), so I've found it a great resource when diving into the Xilinx on-line resources and videos. This resource is very timely ;-)

These tips are absolute gold for a relatively inexperienced FPGA engineer. Definitely worth a read. This book underlines the fact that most often it's small little things that make a huge difference in the success or failure of an FPGA project.

The book is good if you are working with Xilinx and have a Xilinx tool available to try out whatever you are reading. If you want a general guide, then maybe you will have to pick and choose whatever is useful

I've just read a quarter of the book so far. I like the approach of collecting many little pieces of knowledge in a single resource and I like the different topics presented here. It's very practical in the sense that shows you how to implement the techniques and proposed approaches to solve a problem. But at the same time the articles don't dig very deep and sometimes it feels incomplete.

But I like how the articles are organized and the different subjects are non common making it a very interesting book. It would be perfect to have a kindle edition of this so I could read the articles that I'm currently interested on a bus. Very powerful tips. Definitely worth it, I recommend it!

This book provides excellent hand-on power tips for FPGA Designers. Very handy and to the point description of the concepts.

As stated on the back cover, the book is a collection of short articles on various aspects of FPGA design. The book focuses almost exclusively on Xilinx Vertex-6 FPGAs programmed in Verilog, with some mention of the Spartan-6 line.There is no doubt that documentation is needed so designers can learn quickly how to use FPGAs effectively. The vendor documentation (from both Xilinx and Altera) is excellent but so extensive as to be overwhelming. A designer may not know where to start, and may not know the design tricks that will save them a lot of trouble. So, a need exists.Unfortunately, this book does not really fill that need. The fundamental shortcoming of the book is that the articles are overwhelmingly empty of information. To pick some examples at random:Article 25 is "Counters". The article shows Verilog for several counter architectures (binary synchronous, Johnson, LFSR, and cascaded binary synchronous counters). A table lists resource consumption and maximum counting frequency for several implementations, apparently from the Xilinx synthesis tool on the counters alone. The table includes a counter based on a Xilinx multiply-accumulate block, with only a note that the counter is included. There just doesn't seem to be any need for this article, someone designing FPGA logic without knowing how to write a counter is not going to be rescued by this book.Article 40 is "Estimating FPGA power consumption". The article has a short paragraph on each of 3 Xilinx tools for power estimation, huge screenshots, and results from using two of the tools to estimate power for a memory controller. The tool results show an almost 2:1 difference in estimated power (1.4W vs. 2.6W), accounted for by a more than 3:1 difference in estimated I/O power consumption. That is the end of the information. There is no discussion about how the designer might choose between the power estimates. After reading this 4.5 page article, you know only that three Xilinx tools are available, and that their power estimates can differ greatly.Article 71 is "Serial and Parallel CRC". This article describes a method for converting a serial CRC generator to a parallel CRC generator. That method may be useful if you need it. The article appears to be very good.Article 80 is "Design Area Optimizations: Coding Style". This article discusses several topics. The section 'Priority encoders' compares building a priority encoder using '?' operators vs. 'case'. The article explains that the 'case' approach may have better

performance, and presents a table of synthesizer results for '?' vs. 'case'. The table shows logic utilization but leaves out timing information, so I do not know what to make of the performance tradeoff.The book is physically bloated. The text is presented in a 12 point font instead of the usual 10 point, the Verilog samples and the Xilinx tool output are in a very wide 12 point typewriter font. The 5 page index would probably fit on 1 page with normal book design. I would call this a book with 75 pages of information, padded to 200+ pages, then doubled using large fonts and large screenshots.

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